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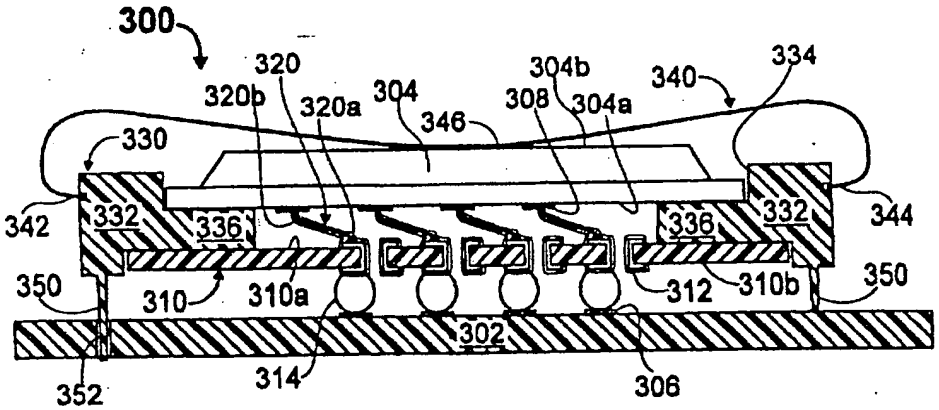

(57) Abstract

Resilient contact structures extend from a top surface of a support substrate and solder-ball (or other suitable) contact structures are disposed on a bottom surface of the support substrate. Interconnection elements (110) are used as the resilient contact structures and are disposed atop the support substrate. Selected ones of the resilient contact structures atop the support substrate are connected, via the support substrate, to corresponding ones of the contact structures on the bottom surface of the support substrate. In an embodiment intended to receive an LGA-type semiconductor package (304), pressure contact is made between the resilient contact structures and external connection points of the semiconductor package with a contact force which is generally normal to the top surface of the support substrate (302). In an embodiment intended to receive a BGA-type semiconductor package (404), pressure contact is made between the resilient contact structures and external connection points of the semiconductor package with a contact force which is generally parallel to the top surface of the support substrate (402).

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MOUNTING ELECTRONIC COMPONENTS TO A CIRCUIT BOARD

TECHNICAL FIELD OF THE INVENTION

The invention relates to making interconnections between electronic components, especially microelectronic components and, more particularly, to providing techniques for removably mounting (socketing) semiconductor dies and packages to circuit boards.

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation-in-part of commonly-owned, copending U.S. Patent Application No. 08/452,255 (hereinafter "PARENT CASE"), filed 5/26/95 (status: pending), which is a continuation-in-part of commonly-owned, copending U.S. Patent Application No. 08/340,144 filed 11/15/94 (status: pending) and its counterpart PCT patent application number PCT/US94/13373 filed 11/16/94 (published 26 May 95 as WO 95/14314), both of which are continuations-in-part of commonly-owned, copending U.S. Patent Application No. 08/152,812, filed 11/16/93 (status: pending/allowed).

This is also a continuation-in-part of commonly-owned, copending U.S. Patent Application No. 08/526,246 filed 9/21/95 (status: pending).

BACKGROUND OF THE INVENTION

Electronic components, particularly microelectronic components such as semiconductor devices (chips), often have a plurality of terminals (also referred to as bond pads, electrodes, or conductive areas). In order to assemble such devices into a useful system (or subsystem), a number of individual devices must be electrically interconnected with one another, typically through the intermediary of a printed circuit (or wiring) board (PCB, PWB).

Semiconductor devices are typically disposed within a semiconductor package having a plurality of external connection points in the form of pins, pads, leads, solder balls, and the like. Many types of semiconductor packages are known, and techniques for connecting the semiconductor device within the package include bond wires, tape-automated bonding (TAB) and the like. In some cases, a semiconductor device is provided with raised bump contacts, and is connected by flip-chip techniques onto another electronic component.

Generally, interconnections between electronic components can be classified into the two broad categories of "relatively permanent" and "readily demountable".

An example of a "relatively permanent" connection is a solder joint. Once two components are soldered to one another, a process of unsoldering must be used to separate the components. A wire bond is another example of a "relatively permanent" connection.

An example of a "readily demountable" connection is rigid pins of one electronic component being received by resilient socket elements of another electronic component. The socket elements exert a contact force (pressure) on the pins in an

amount sufficient to ensure a reliable electrical connection therebetween. Interconnection elements intended to make pressure contact with an electronic component are referred to herein as "springs" or "spring elements".

Spring elements are well known, and appear in a variety of shapes and sizes. In today's microelectronic environment, there is a profound need for all interconnection elements, including springs, to become smaller and smaller, in order that a large plurality of such interconnection elements can be disposed in a small area, to effect a high density of interconnections to electronic components.

Prior art techniques for making spring elements generally involve stamping (punching) or etching a spring material, such as phosphor bronze or beryllium copper or steel or a nickel-iron-cobalt (e.g., kovar) alloy, to form individual spring elements, shaping the spring elements to have a spring shape (e.g., arcuate, etc.), plating the spring elements with a good contact material (e.g., a noble metal such as gold, which will exhibit low contact resistance when contacting a like material), and molding a plurality of such shaped, plated spring elements into a linear, a peripheral or an array pattern. When plating gold onto the aforementioned materials, sometimes a thin (for example, 30-50 microinches), barrier layer of nickel is appropriate.

Various problems and limitations are inherent with such techniques of making spring elements.

For example, these processes are limited when applications demand that a plurality of springs (interconnection elements) be arranged at a fine (e.g., 10 mil) pitch. Such a fine pitch inherently demands that each spring be sized (i.e., in cross-section) substantially smaller (e.g., 3 mil) than the pitch.

A punch-out area must be accommodated, and will limit how much material is left over to form springs. At best, even through it may be relatively straightforward to punch out springs as small as 1 mil, such small sizes impose limitations on the contact force that can reliably be exerted by the springs. This is especially poignant in the context of fabricating area arrays of springs.

Generally, a certain minimum contact force is desired to effect reliable pressure contact to electronic components (e.g., to terminals on electronic components). For example, a contact (load) force of approximately 15 grams (including as little as 2 grams or less and as much as 150 grams or more, per contact) may be desired to ensure that a reliable electrical connection is made to a terminal of an electronic component which may be contaminated with films on its surface, or which has corrosion or oxidation products on its surface. The minimum contact force required of each spring demands either that the yield strength of the spring material or that the size of the spring element are increased. As a general proposition, the higher the yield strength of a material, the more difficult it will be to work with (e.g., punch, bend, etc.). And the desire to make springs smaller essentially rules out making them larger in cross-section.

Another limitation attendant prior art interconnection elements is that when hard materials (such as would be used for making springs) are employed, relatively "hostile" (e.g., high temperature) processes such as brazing are required to mount the interconnection elements to terminals of an electronic component. For example, it is known to braze rigid pins to relatively "durable" semiconductor packages. Such "hostile" processes are generally not desirable (and often not feasible) in the context of certain relatively "fragile" electronic components such as semiconductor devices. In contrast thereto,

wire bonding is an example of a relatively "friendly" processes which is much less potentially damaging to fragile electronic components than brazing. Soldering is another example of a relatively "friendly" process.

Another problem associated with mounting springs on electronic components is largely mechanical in nature. In cases where a spring is mounted at one end to a substrate (which, for purposes of this proposition is considered to be an immovable object), and is required to react forces applied at its free end, the "weak link" (weakest point, in service) will often be the point at which the spring is attached (e.g., the base of the spring is bonded) to the substrate (e.g., terminal of an electronic component). This accounts, at least in part, for the requirement to employ "hostile" processes (e.g., brazing) to mount the springs to the substrate.

Another subtle problem associated with interconnection elements, including spring contacts, is that, often, the terminals of an electronic component are not perfectly coplanar. Interconnection elements lacking in some mechanism incorporated therewith for accommodating these "tolerances" (gross non-planarities) will be hard pressed to make consistent contact pressure contact with the terminals of the electronic component.

In many modern electronic systems, one or more packaged semiconductor devices are mounted to circuit boards. Various packaging types are well known. Generally, all semiconductor packages have external connections which are either pins, pads, leads, ball bumps, or the like.

One type of semiconductor package is typified by USP 4,700,276 ("FREYMAN"), entitled ULTRA HIGH DENSITY PAD ARRAY CHIP CARRIER. As generally disclosed therein, a ceramic substrate is provided with a plurality of through holes plugged

with solder on its bottom surface. These solder plugs (206) are arranged in an array pattern, and form external surface mount interconnection points for the final chip carrier arrangement. The solder plugs are generally hemispherical, and permit the substrate to sit high above the board to which the carrier is mounted. A semiconductor package having an array of solder balls as its interconnection points on an external surface thereof is referred to herein as a Ball Grid Array (BGA) type package.

Generally, BGA solder balls are of two types: (1) eutectic masses that melt upon reflow; and (2) masses such as of 90:10 lead:tin that are not melted, but rather are attached with a eutectic material. The first type of solder ball will collapse slightly (e.g., approximately 6 mils) upon reflow, resulting in some concern over the final planarity of the plurality of connections effected thereby. The second type of solder ball does not collapse, since they are not reflowed. However, since a eutectic material is employed to attach the second type of solder balls, certain substrate materials that cannot withstand the heat associated with eutectic attach processes cannot be employed. This information is provided for general background purposes.

Another type of semiconductor package is the Land Grid Array (LGA), which is provided with a plurality (e.g., an array) of terminals (contact pads (or "lands") on a surface thereof. Generally, resilient interconnection elements are used to make electrical connections to the lands of an LGA. The present invention discloses a "socket" having a plurality of resilient interconnection elements for making electrical connections to the terminals of an electronic component such as an LGA-type semiconductor package.

It is generally desired that sockets for LGA and BGA type

semiconductor packages be soldered down (e.g., surface-mounted) to a circuit board. Prior art sockets relying on pins require corresponding holes through the circuit board. Using conventional techniques of fabricating holes (e.g., plated through holes) in circuit boards, spacing between adjacent holes (pitch) is typically constrained to no less than 100 mils between adjacent holes. Moreover, plated through holes represent an additional cost in the manufacture of circuit boards. What is needed is a "solder-down" or "surface-mountable" socket to permit connections to be made at a finer pitch (e.g., 50 mils) and at reduced cost.

Additional references of interest, vis-a-vis BGA and LGA type packages include the following US Patents: 5,241,133; 5,136,366; 5,077,633; 5,006,673; and 4,700,473.

The aforementioned BGA type package is surface-mounted, by soldering the semiconductor package down onto a PCB. This effects a more-or-less permanent connection of the packaged semiconductor device to the PCB. In order to remove the packaged semiconductor device (such as for replacement or upgrading), it would be necessary to unsolder the entire package from the PCB - a process which can damage either the PCB or the semiconductor device contained within the semiconductor package. Moreover, in order to unsolder a component from a PCB, it is generally necessary to remove the PCB from the system in which it is located.

Techniques for demountably connecting semiconductor packages to PCBs do not suffer from such vagaries. For example, a semiconductor package having pins is readily plugged into a socket which is permanently mounted to a PCB, and is just as readily removed from the socket.

One aspect of the present invention is directed to

providing a technique whereby any electronic component such as a BGA or an LGA type semiconductor package can readily be demounted, without unsoldering, from a PCB - in other words, providing "sockets" for BGA and LGA type semiconductor packages. This facilitates not only the replacement/upgrading of the packaged semiconductor device, but also provides the opportunity to test the packaged semiconductor device in instances where the PCB is a probe card, or a probe card insert.

As a general proposition, demountable connections require some sort of pressure contact to be made between electronic components. Sockets for receiving pinned semiconductor packages typically have leaf-type spring elements for receiving the package pins.

The following U.S. Patents are cited as being of interest: 5,386,344; 5,336,380; 5,317,479; 5,086,337; 5,067,007; 4,989,069; 4,893,172; 4,793,814; 4,777,564; 4,764,848; 4,667,219; 4,642,889; 4,330,165; 4,295,700; 4,067,104; 3,795,037; 3,616,532; and 3,509,270.

Another aspect of the present invention is directed to techniques for forming solder balls and/or raised solder bumps on electronic components, particularly on chip carriers or semiconductor packages. In the main hereinafter, techniques for forming solder "balls" are discussed.

Techniques for forming solder balls and/or raised solder bumps on electronic components include, by way of example only:

(1) applying dollops (small quantities) of solder paste to contact pads and reflowing the solder paste;

(2) solder-plugging plated areas (see, e.g., Figure 2c of FREYMAN);

(3) molding solder ball contacts directly on a substrate (see, e.g., USP 5,381,848); and

(4) filling holes in a film carrier with solder, placing the carrier over the substrate, and reflowing the solder to adhere to contact pads on the substrate (see, e.g., USP 5,388,327).

Other methods of forming raised solder contacts, of some relevance to the present invention, are the techniques disclosed in the aforementioned commonly-owned, copending U.S. Patent Applications Nos. 08/152,812, 08/340,144 and 08/452,255, which generally involve bonding a wire at two (both) ends to a terminal of an electronic component and overcoating the wire with solder. (See, e.g., Figures 24A and 24B of 08/452,255; Figure 16 of 08/340,144; and Figures 2-5 of 08/152,812.)

BRIEF DESCRIPTION (SUMMARY) OF THE INVENTION

It is a general object of the present invention to provide a technique for fabricating interconnection elements for electronic components.

It is another object of the invention to provide interconnection elements that attach easily to electronic components.

It is another object of the invention to provide interconnection elements that are suitable for making pressure contact to electronic components.

It is another object of the invention to provide a technique for demountably interconnecting (socketing) a BGA-type semiconductor package to an electronic component, such as a PCB.

It is another object of the invention to provide a technique for demountably interconnecting (socketing) an LGA-type semiconductor package to an electronic component, such as a PCB.

It is another object of the invention to provide a technique for forming solder balls and/or raised solder bumps on electronic components, particularly on chip carriers or semiconductor packages.

According to the invention, techniques are disclosed for fabricating interconnection elements, particularly spring elements, and for mounting the interconnection elements to electronic components. The disclosed techniques overcome problems associated with making spring elements of extremely small size, yet capable of exerting contact forces of sufficient

magnitude to ensure reliable interconnections. The disclosed techniques also overcome problems associated with mounting springs on electronic components, such as semiconductor devices.

According to the invention, a "composite" (multilayer) interconnection element is fabricated by mounting an elongate element ("core") to an electronic component, shaping the core to have a spring shape, and overcoating the core to enhance the physical (e.g., spring) characteristics of the resulting composite interconnection element and/or to securely anchor the resulting composite interconnection element to the electronic component.

The use of the term "composite", throughout the description set forth herein, is consistent with a 'generic' meaning of the term (e.g., formed of two or more elements), and is not to be confused with any usage of the term "composite" in other fields of endeavor, for example, as it may be applied to materials such as glass, carbon or other fibers supported in a matrix of resin or the like.

As used herein, the term "spring shape" refers to virtually any shape of an elongate element which will exhibit elastic (restorative) movement of an end (tip) of the elongate element with respect to a force applied to the tip. This includes elongate elements shaped to have one or more bends, as well as substantially straight elongate elements.

As used herein, the terms "contact area", "terminal", "pad", and the like refer to any conductive area on any electronic component to which an interconnection element is mounted or makes contact.

As used herein, the term "solder ball" refers to any mass of solder, or the like, providing a solderable, raised contact

structure on a surface of an electronic component such as a semiconductor package or a support substrate. Such solder balls are employed to make permanent electrical connections between the electronic component to which they are mounted and terminals of another electronic component.

Alternatively, the core is shaped prior to mounting to an electronic component.

Alternatively, the core is mounted to or is a part of a sacrificial substrate which is not an electronic component. The sacrificial substrate is removed after shaping, and either before or after overcoating. According to an aspect of the invention, tips having various topographies can be disposed at the contact ends of the interconnection elements. (See also Figures 11A-11F of the aforementioned PARENT CASE.)

In an embodiment of the invention, the core is a "soft" material having a relatively low yield strength, and is overcoated with a "hard" material having a relatively high yield strength. For example, a soft material such as a gold wire is attached (e.g., by wire bonding) to a bond pad of a semiconductor device and is overcoated (e.g., by electrochemical plating) with a hard material such nickel and its alloys.

Vis-a-vis overcoating the core, single and multi-layer overcoatings, "rough" overcoatings having microprotrusions (see also Figures 5C and 5D of the PARENT CASE), and overcoatings extending the entire length of or only a portion of the length of the core, are described. In the latter case, the tip of the core may suitably be exposed for making contact to an electronic component (see also Figure 5B of the PARENT CASE).

Generally, throughout the description set forth herein, the term "plating" is used as exemplary of a number of

techniques for overcoating the core. It is within the scope of this invention that the core can be overcoated by any suitable technique including, but not limited to: various processes involving deposition of materials out of aqueous solutions; electrolytic plating; electroless plating; chemical vapor deposition (CVD); physical vapor deposition (PVD); processes causing the deposition of materials through induced disintegration of liquid or solid precursors; and the like, all of these techniques for depositing materials being generally well known.

Generally, for overcoating the core with a metallic material such as nickel, electrochemical processes are preferred, especially electroless plating.

In another embodiment of the invention, the core is an elongate element of a "hard" material, inherently suitable to functioning as a spring element, and is mounted at one end to a terminal of an electronic component. The core, and at least an adjacent area of the terminal, is overcoated with a material which will enhance anchoring the core to the terminal. In this manner, it is not necessary that the core be well-mounted to the terminal prior to overcoating, and processes which are less potentially damaging to the electronic component may be employed to "tack" the core in place for subsequent overcoating. These "friendly" processes include soldering, gluing, and piercing an end of the hard core into a soft portion of the terminal.

Embodiments wherein the core is a wire are disclosed. Embodiments wherein the core is a flat tab (conductive metallic ribbon) are also disclosed.

Representative materials, both for the core and for the overcoatings, are disclosed.

In the main hereinafter, techniques involving beginning with a relatively soft (low yield strength) core, which is generally of very small dimension (e.g., 3.0 mil or less) are described. Soft materials, such as gold, which attach easily to semiconductor devices, generally lack sufficient resiliency to function as springs. (Such soft, metallic materials exhibit primarily plastic, rather than elastic deformation.) Other soft materials which may attach easily to semiconductor devices and possess appropriate resiliency are often electrically non-conductive, as in the case of most elastomeric materials. In either case, desired structural and electrical characteristics can be imparted to the resulting composite interconnection element by the overcoating applied over the core. The resulting composite interconnection element can be made very small, yet can exhibit appropriate contact forces. Moreover, a plurality of such composite interconnection elements can be arranged at a fine pitch (e.g., 10 mils), even though they have a length (e.g., 100 mils) which is much greater than the distance to a neighboring composite interconnection element (the distance between neighboring interconnection elements being termed "pitch").

It is within the scope of this invention that composite interconnection elements can be fabricated on a microminiature scale, for example as "microsprings" for connectors and sockets, having cross-sectional dimensions on the order of twenty-five microns (μm), or less. This ability to manufacture reliable interconnection having dimensions measured in microns, rather than mils, squarely addresses the evolving needs of existing interconnection technology and future area array technology.

The composite interconnection elements of the present invention exhibit superior electrical characteristics, including electrical conductivity, solderability and low contact resistance. In many cases, deflection of the interconnection

element in response to applied contact forces results in a "wiping" contact, which helps ensure that a reliable contact is made.

An additional advantage of the present invention is that connections made with the interconnection elements of the present invention are readily demountable. Soldering, to effect the interconnection to a terminal of an electronic component is optional, but is generally not preferred at a system level.

According to an aspect of the invention, techniques are described for making interconnection elements having controlled impedance. These techniques generally involve coating (e.g., electrophoretically) a conductive core or an entire composite interconnection element with a dielectric material (insulating layer), and overcoating the dielectric material with an outer layer of a conductive material. By grounding the outer conductive material layer, the resulting interconnection element can effectively be shielded, and its impedance can readily be controlled. (See also Figure 10K of the PARENT CASE.)

According to an aspect of the invention, interconnection elements can be pre-fabricated as individual units, for later attachment to electronic components. Various techniques for accomplishing this objective are set forth herein. Although not specifically covered in this document, it is deemed to be relatively straightforward to fabricate a machine that will handle the mounting of a plurality of individual interconnection elements to a substrate or, alternatively, suspending a plurality of individual interconnection elements in an elastomer, or on a support substrate.

It should clearly be understood that the composite interconnection element of the present invention differs dramatically from interconnection elements of the prior art

which have been coated to enhance their electrical conductivity characteristics or to enhance their resistance to corrosion.

The overcoating of the present invention is specifically intended to substantially enhance anchoring of the interconnection element to a terminal of an electronic component and/or to impart desired resilient characteristics to the resulting composite interconnection element. Stresses (contact forces) are directed to portions of the interconnection elements which are specifically intended to absorb the stresses.

It should also be appreciated that the present invention provides essentially a new technique for making spring structures. Generally, the operative structure of the resulting spring is a product of plating, rather than of bending and shaping. This opens the door to using a wide variety of materials to establish the spring shape, and a variety of "friendly" processes for attaching the "falsework" of the core to electronic components. The overcoating functions as a "superstructure" over the "falsework" of the core, both of which terms have their origins in the field of civil engineering.

According to one aspect of the present invention, "sockets" are provided for permitting LGA and BGA type semiconductor packages to be removably connected (socketed) to an electronic component such as a circuit board (e.g., PCB, PWB). Generally, the sockets include a support substrate having a top surface and a bottom surface. Solder balls, or the like, are provided on the bottom surface of the support substrate for soldering the socket to a circuit board, thereby effecting a permanent (albeit demountable) connection between the socket and a circuit board (hence, the term "solder-down", as used herein). A plurality of resilient contact structures are provided on the top surface of the support substrate (or in any suitable manner permitting the resilient contact structures to extend upward from the top

surface of the support substrate) for making pressure connections to the external connection points (pads, balls) of an LGA-type or of a BGA-type package, respectively.

Generally, throughout the socket embodiments disclosed herein, any resilient contact structure may be used. The composite interconnection elements of the present invention are simply an example of suitable resilient contact structures for such sockets, and are generally preferred due to their aforementioned relative ease of manufacture with small dimensions.

In an embodiment of the invention serving as a socket for LGA-type packages, the pressure contact is made to tips of the resilient contact structures in a direction which is generally normal to the top surface of the support substrate.

In an embodiment of the invention serving as a socket for BGA-type packages, the pressure contact is made to tips of the resilient contact structures in a direction which is generally parallel to the top surface of the support substrate.

Generally, the embodiments of solder-down sockets described herein provide an effective technique for making pressure connections to terminals of any electronic component, including semiconductor packages and bare unpackaged semiconductor dies. The solder-down socket includes a support substrate having a top surface and a bottom surface, a plurality of resilient contact structures extending from the top surface of the support substrate, each resilient contact structure having a tip at a free end thereof; and means for effecting a pressure connection between the tips of the resilient contact structures and the terminals of the electronic component. Generally, either one or the other of the electronic component or the tips of the resilient contact structures must be moved, relative to the other, to effect such pressure connections. For example,

the means for effecting the pressure connection may be a movable sliding element to which the electronic component is mounted, suitable for moving the terminals of the electronic component against the tips of the resilient contact structures. Alternatively, the means for effecting the pressure connection may be a movable sliding element acting upon the resilient contact structures, suitable for moving the tips of the resilient contact structures against the terminals of the electronic component. In either case, it is desirable to effect a wiping movement of the tips of the resilient contact structures against the terminals of the electronic component. Preferably, irrespective of whether it is the tips of the resilient contact structures or the terminals themselves that are moved, a mechanism is provided for limiting how far the tips of the resilient contact structures across the terminals of the electronic component, to ensure that they remain in pressure contact with the terminals of the electronic component. As noted, it is preferred that the socket be permanently mounted to a circuit board. To this end, it is preferred that a plurality of solderable raised contact structure are disposed on the bottom surface of the support substrate and connected via the support substrate to the plurality of resilient contact structures.

It should be understood that the LGA-type sockets disclosed herein are suitable for making pressure connections to bare dies having bond pads disposed on a surface thereof, and that the BGA type sockets disclosed herein are suitable for making pressure connections to bare dies having raised contact structures disposed on a surface thereof. An example of raised contact structures on a surface of a semiconductor die are raised solder contacts (bumps) fabricated by IBM's "C4" process. As used herein, a "bare die" is a semiconductor chip (device) that has not been packaged, whether the chip is aggregated with other chips on a semiconductor wafer or after individual chips have

been singulated from a semiconductor wafer.

Additionally, a novel technique is disclosed for mounting solder balls on pads (contact areas, terminals) of an electronic component. For example, this technique can be employed to mount the aforementioned solder balls on the aforementioned support substrates for LGA and BGA solder-down sockets.

Generally, the solder preform includes a plurality of large solder masses connected to one another by a plurality of smaller solder bridges. The solder preform is disposed against a surface of an electronic component whereupon it is desired to mount solder balls, and the solder preform is heated so as to reflow the solder masses and solder bridges. During reflow, the solder masses become solder balls, and the solder bridges are subsumed into the solder balls. Preferably, soldering flux or solder paste is provided on either the solder preform or on the pads of the electronic component prior to reflow heating.

Other objects, features and advantages of the invention will become apparent in light of the following description thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference will be made in detail to preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Although the invention will be described in the context of these preferred embodiments, it should be understood that it is not intended to limit the spirit and scope of the invention to these particular embodiments.

Figure 1A is a cross-sectional view of a longitudinal portion, including one end, of an interconnection element, according to an embodiment of the invention.

Figure 1B is a cross-sectional view of a longitudinal portion, including one end, of an interconnection element, according to another embodiment of the invention.

Figure 1C is a cross-sectional view of a longitudinal portion, including one end of an interconnection element, according to another embodiment of the invention.

Figure 1D is a cross-sectional view of a longitudinal portion, including one end of an interconnection element, according to another embodiment of the invention.

Figure 1E is a cross-sectional view of a longitudinal portion, including one end of an interconnection element, according to another embodiment of the invention.

Figure 2A is a cross-sectional view of an interconnection element mounted to a terminal of an electronic component and having a multi-layered shell, according to the invention.

Figure 2B is a cross-sectional view of an interconnection element having a multi-layered shell, wherein an intermediate

layer is of a dielectric material, according to the invention.

Figure 2C is a perspective view of a plurality of interconnection elements mounted to an electronic component (e.g., a probe card insert), according to the invention.

Figure 2D is a cross-sectional view of an exemplary first step of a technique for manufacturing interconnection elements, according to the invention.

Figure 2E is a cross-sectional view of an exemplary further step of the technique of **Figure 2D** for manufacturing interconnection elements, according to the invention.

Figure 2F is a cross-sectional view of an exemplary further step of the technique of **Figure 2E** for manufacturing interconnection elements, according to the invention.

Figure 2G is a cross-sectional view of an exemplary plurality of individual interconnection elements fabricated according to the technique of **Figures 2D-2F**, according to the invention.

Figure 2H is a cross-sectional view of an exemplary plurality of interconnection elements fabricated according to the technique of **Figures 2D-2F**, and associated in a prescribed spatial relationship with one another, according to the invention.

Figure 2I is a cross-sectional view of an alternate embodiment for manufacturing interconnection elements, showing a one end portion of one interconnection element, according to the invention.

Figure 3 is a cross-sectional view of an embodiment of an

LGA socket, according to the invention.

Figure 3A is a cross-sectional view of another embodiment of an LGA socket, according to the invention.

Figure 3B is a cross-sectional view of another embodiment of a socket, showing a one end portion of one interconnection element, according to the present invention.

Figure 3C is a cross-sectional view of another embodiment of a socket, showing a one end portion of one interconnection element, according to the present invention.

Figure 4 is a cross-sectional view of an embodiment of a BGA socket, according to the invention.

Figure 4A is a cross-sectional view of another embodiment of a BGA socket, according to the invention.

Figure 4B is a top view, partially in cross-section, of an interconnection element making contact to a solder ball, according to the invention.

Figure 4C is a cross-sectional view of another embodiment of a BGA socket, according to the invention.

Figure 4D is a cross-sectional view of another embodiment of a BGA socket, according to the invention.

Figure 5A is a top view, partially in cross-section, of an interconnection element making contact to a solder ball, according to an alternate embodiment of the invention.

Figure 5B is a perspective view of a portion of an LGA

socket, according to an alternate embodiment of the invention.

Figure 5C is a cross-sectional view of a portion of an alternate embodiment of a solder-down socket, according to the present invention.

Figure 5D is a cross-sectional view of a portion of an alternate embodiment of a solder-down socket, according to the present invention.

Figure 6A is a perspective view of a technique for mounting pairs of interconnection elements as interconnection structures to a substrate, according to the invention.

Figure 6B is a perspective view of another technique for mounting pairs of interconnection elements as interconnection structures to a substrate, according to the invention.

Figure 6C is a top plan view of a pair of interconnection elements contacting terminal of an electronic component (e.g., an external ball bump connection of a semiconductor package), according to the invention.

Figure 6D is a side view of an interconnection element making contact to a ball bump terminal of an electronic component, according to another embodiment of the invention.

Figure 6E is a side view of an interconnection element making contact to a ball bump terminal of an electronic component, according to another embodiment of the invention.

Figure 7A is a perspective view, partially in cross-section, of a solder preform for use in attaching a plurality of ball bump type terminals to an electronic component, according to another aspect of the invention.

Figure 7B is a side, cross-sectional view of the solder preform of **Figure 7A**, in a subsequent step of the technique of attaching ball bumps to an electronic component, according to the invention.

Figure 7C is a side view, partially in cross-section, of ball bump terminals mounted to an electronic component, according to the invention.

CLAIMS

What is claimed is:

1. Method of removably connecting an electronic component to a circuit board, said circuit board having a plurality of contact areas on a surface thereof, said electronic component having a plurality of terminals on a surface thereof, comprising:

disposing a support substrate between the electronic component and the circuit board, the support substrate having a top surface and a bottom surface opposite the top surface;

mounting a plurality of resilient contact structures to the top surface of the support substrate;

mounting a plurality of contact structures to the bottom surface of the support substrate;

mounting the support substrate to the circuit board so as to make permanent electrical connections between the contact structures and the contact areas;

urging the electronic component against the resilient contact structures so that removable connections are made between the plurality of terminals and the resilient contact structures; and

within the support substrate, interconnecting selected ones of the resilient contact structures with selected ones of the contact structures.

2. Method, according to claim 1, further comprising:

fabricating the resilient contact structures as composite interconnection elements.

3. Method, according to claim 1, further comprising:

forming the contact structures as solder balls.

4. Method, according to claim 1, further comprising:

soldering the contact structures to the contact areas

5. Method, according to claim 1, wherein:

the electronic component is selected from the group consisting of LGA-type semiconductor package, BGA-type semiconductor package and bare semiconductor die.

6. Method, according to claim 1, wherein:

each of the resilient contact structures has a tip; and

the terminals are urged against the tips of the resilient contact structures in a direction which is generally normal to the top surface of the support substrate.

7. Method, according to claim 1, wherein:

each of the resilient contact structures has a tip; and

when the terminals are urged against the tips of the resilient contact structures in a first direction which is generally normal to the top surface of the support substrate, the tips deflect in the first direction to effect a pressure connection between the tips and the terminals and move in a second direction which is generally parallel to the top surface of the support substrate so as to wipe across the pads.

8. Method, according to claim 1, wherein:

each of the resilient contact structures has a tip; and

the terminals are urged against tips of the resilient contact structures in a direction which is generally parallel to the top surface of the support substrate.

9. Solder-down socket, comprising:

a support substrate;

a plurality of resilient contact structures extending upward from a top surface of the support substrate; and

a plurality of solderable raised contact structures disposed on a bottom surface of the substrate, said solderable raised contact structures being electrically connected to the resilient contact structures.

10. Socket, according to claim 9, further comprising:

means for urging an electronic component against tips of the resilient contact structures.

11. Socket, according to claim 10, wherein:

the electronic component is selected from the group consisting of LGA-type semiconductor package, BGA-type semiconductor package and bare semiconductor die.

12. Socket, according to claim 9, wherein:

the resilient contact structures are mounted to the top surface of the support substrate.

13. Socket, according to claim 9, wherein:

end portions of the resilient contact structures extend at least into the support substrate.

14. Socket, according to claim 13, wherein:

the end portions of the resilient contact structures extend through the support substrate.

15. Socket, according to claim 13, wherein:

the solderable raised contact structures are directly connected to ends of the resilient contact structures.

16. Socket, according to claim 13, further comprising:

a plurality of plated through holes extending through the support substrate;

wherein:

the end portions of the resilient contact structures extend into the plated through holes.

17. Socket for releasably connecting an electronic component to a circuit board, comprising:

resilient contact structures extending upward from a top surface of a support substrate

contact structures disposed on a bottom surface of the support substrate and connected through the support substrate to the resilient contact structures.

18. Socket, according to claim 17, wherein:

the resilient contact structures are composite interconnection elements

19. Socket, according to claim 17, further comprising:

a frame element disposed around a peripheral edge of the support substrate.

20. Socket, according to claim 19, further comprising:

means for aligning the frame element in a prescribed positional relationship to the circuit board.

21. Socket, according to claim 20, wherein the means for aligning includes pins extending from the frame element and corresponding holes in the circuit board.

22. Socket, according to claim 17, wherein:

the resilient contact structures are formed as cantilever beams.

23. Socket, according to claim 17, wherein:
the contact structures are solder balls.

24. Socket, according to claim 17, wherein:
each of the resilient contact structures has a tip; and
further comprising:
a stiffener element disposed above the support substrate having holes through which the tips of the resilient contact structures extend.

25. Socket, according to claim 17, further comprising:
means for urging the electronic component down onto the tips of the resilient contact structures.

26. Socket, according to claim 25, wherein the means for urging includes a spring clip which extends across a top surface of the frame element.

27. Socket, according to claim 17, further comprising:
means for receiving the electronic component on an upper surface thereof, and for permitting the resilient contact structures to make pressure contact with the external connection points of the electronic component, said means for receiving the electronic component having a lower surface opposing the top surface of the support substrate.

28. Socket, according to claim 27, wherein the means for receiving the electronic component is a planar element.

29. Socket, according to claim 28, further comprising:
a plurality of holes extending through the planar element, from the upper surface to the lower surface thereof.

30. Socket, according to claim 29, wherein:

said holes are tapered and have a smaller dimension at the upper surface of the planar element and a larger dimension at the lower surface of the planar element.

31. Socket, according to claim 28, further comprising:

means for moving the planar element in a direction parallel to the top surface of the support substrate to provide an effective pressure contact between the external connection points and the resilient contact structures.

32. Socket, according to claim 17, further comprising:

a frame element disposed around the support substrate;

a planar element disposed above the support substrate, and having at least one hole permitting the tips of the resilient contact structures to pass through the planar element;

a cam lever extending from a cavity in the frame element; and

an offset portion of the cam lever extending through a hole in the planar element.

33. Socket, according to claim 32, further comprising:

at least one recess on an inner surface of the frame element, slidably receiving the planar element.

34. Socket, according to claim 32, wherein:

the resilient contact structures are composite interconnection elements.

35. Socket, according to claim 32, wherein:

the contact structures are solder balls.

36. Socket, according to claim 28, further comprising:

means disposed on the upper surface of the planar element for retaining the electronic component.

37. Socket, according to claim 36, wherein:

the means for retaining is at least three pawls extending upward from the upper surface of the planar element.

38. Socket, according to claim 17, wherein:

the electronic component is selected from the group consisting of LGA-type semiconductor package, BGA-type semiconductor package and bare semiconductor die.

39. Solder-down socket, for making pressure connections to terminals of an electronic component, comprising:

a support substrate having a top surface and a bottom surface;

a plurality of resilient contact structures extending from the top surface of the support substrate, each resilient contact structure having a tip at a free end thereof; and

means for effecting a pressure connection between the tips of the resilient contact structures and the terminals of the electronic component.

40. Solder-down socket, according to claim 39, further comprising:

a plurality of solderable raised contact structure disposed on the bottom surface of the support substrate and connected via the support substrate to the plurality of resilient contact structures.

41. Solder-down socket, according to claim 39, wherein:

the means for effecting a pressure connection moves the terminals of the electronic component against the tips of the resilient contact structures.

42. Solder-down socket, according to claim 39, wherein:

the means for effecting a pressure connection moves the tips of the resilient contact structures against the terminals of the electronic component.

43. Solder-down socket, according to claim 39, further comprising:

means for limiting wiping of the tips of the resilient contact structures across the terminals of the electronic component.

44. Solder-down socket, according to claim 39, wherein:

the electronic component is a bare semiconductor die.

45. Solder-down socket, comprising:

a support substrate having a plurality of holes extending therethrough;

a plurality of pre-fabricated resilient contact structures, each having a base portion and a tip;

the resilient contact structures being supported within the holes in a prescribed spatial relationship with one another by the support substrate; and

a solderable raised contact structure disposed on the base portion of each resilient contact structure.

46. Solder-down socket, according to claim 45, wherein:

the resilient contact structures are composite interconnection elements.

47. Solder-down socket, comprising:

a support substrate having a top surface, a bottom surface and a plurality of holes extending therethrough;

a plurality of metallic pads, each pad having a top surface and a bottom surface, each pad disposed on the bottom surface of the support substrate in alignment with a hole;

a plurality of pre-fabricated resilient contact structures, each having a base portion and a tip;

the base portions of the resilient contact structures being supported in a prescribed spatial relationship with one another by the top surfaces of the metallic pads; and

a solderable raised contact structure disposed on the bottom surface of each metallic pad.

48. Solder-down socket, according to claim 47, wherein:

the resilient contact structures are composite interconnection elements.

49. Interconnection structure for making contact to first terminals of an electronic component, comprising:

a support substrate having a top surface and second terminals disposed on the top surface of the substrate; and

a plurality of resilient contact structures extending generally parallel to one another from each second terminal, the resilient contact structures extending from each second terminal acting in concert with one another to make a pressure connection to a selected one of the first terminals of the electronic component.

50. Interconnection structure, according to claim 49, wherein:

each resilient contact structure has a tip; and

the tips are oriented to make pressure contact with the first terminals of the electronic component with a contact force that is principally generally normal to the top surface of the support substrate.

51. Interconnection structure, according to claim 49, wherein:

each resilient contact structure has a tip; and

the tips are oriented to make pressure contact with

the first terminals of the electronic component with a contact force that is generally parallel to the top surface of the support substrate.

52. Interconnection element for making contact to terminals of an electronic component, comprising:

a support substrate having a top surface; and

a plurality of resilient contact structures extending from the top surface of the support substrate, each resilient contact structure having two ends, both ends of each resilient contact structure being attached to the support substrate, a midportion of each resilient contact structure shaped to receive a one of the terminals of the electronic component by pressure contact therewith in a direction which is generally parallel to the top surface of the support substrate.

53. Interconnection element, according to claim 52, wherein:

the electronic component is selected from the group consisting of LGA-type semiconductor package, BGA-type semiconductor package and bare semiconductor die.

54. Interconnection element for making contact to terminals of an electronic component, comprising:

a support substrate having a top surface; and

a plurality of resilient contact structures extending from the top surface of the support substrate, each resilient contact structure having a one end attached to the support substrate and an other end extending above the support substrate, an end portion at the other end of the resilient contact structure shaped in an arcuate manner to receive a terminal of the electronic component by pressure contact therewith in a direction which is generally normal to the top surface of the support substrate.

55. Interconnection element, according to claim 54, wherein:

the electronic component is selected from the group consisting of LGA-type semiconductor package, BGA-type semiconductor package and bare semiconductor die.

56. Solder-down socket, comprising:

a circuit board substrate having a plurality of plated through holes extending through the substrate from a top surface to a bottom surface thereof, each through hole having a top contact area exposed on the top surface of the substrate and a bottom contact area exposed on the bottom surface of the substrate;

a plurality of resilient contact structures mounted to the top contact areas and extending from the top surface of the substrate; and

a plurality of solder balls mounted to the bottom contact areas of the plated through holes.

57. Solder-down socket, comprising:

a support substrate having a plurality of plated through holes extending through the substrate from a top surface to a bottom surface thereof, each through hole having a bottom contact area exposed on the bottom surface of the substrate;

a plurality of resilient contact structures mounted into the plated through holes and extending from the top surface of the substrate; and

a plurality of solder balls mounted to the bottom contact areas of the plated through holes.

58. Solder-down socket, comprising:

a support substrate having a plurality of holes extending through the substrate from a top surface to a bottom surface thereof;

a plurality of resilient contact structures having bottom ends mounted in the holes and top ends extending from the top surface of the substrate; and

a plurality of solder balls mounted to the bottom ends of the resilient contact structures.

59. Solder-down socket, according to claim 58, wherein:

the bottom ends of the resilient contact structures extend completely through the holes, end portions thereof being exposed beneath the bottom surface of the support substrate; and

the solder balls are mounted to the end portions of the resilient contact structures

60. Solder-down socket, comprising:

a support substrate having a top surface and a bottom surface;

a plurality of compliant contact structures extending from the top surface of the support substrate; and

a plurality of solder balls mounted to the bottom surface of the support substrate and connected to the compliant

contact structures.

61. Surface-mount socket, comprising:

a support substrate having a top surface and a bottom surface;

a plurality of compliant contact structures extending from the top surface of the support substrate; and

a plurality of solder balls mounted to the bottom surface of the support substrate and connected to the compliant contact structures.

Figure 1A

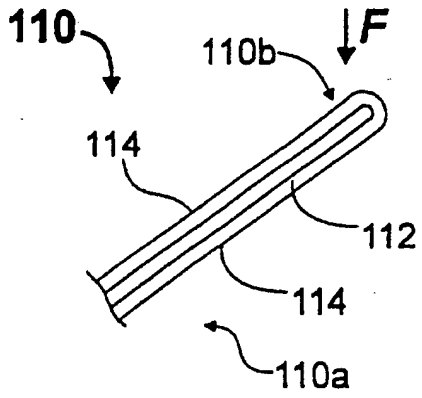


Figure 1B

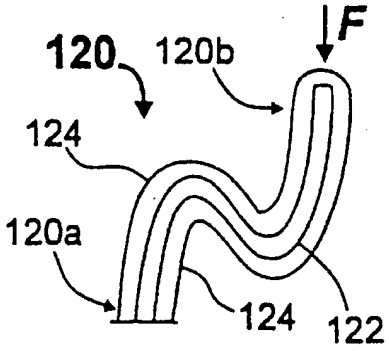


Figure 1C

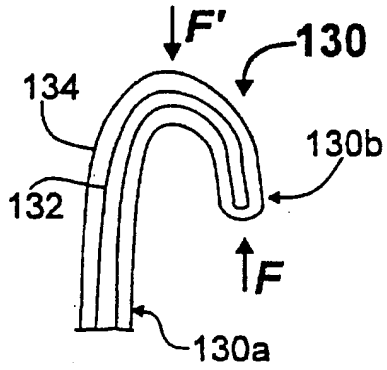


Figure 1D

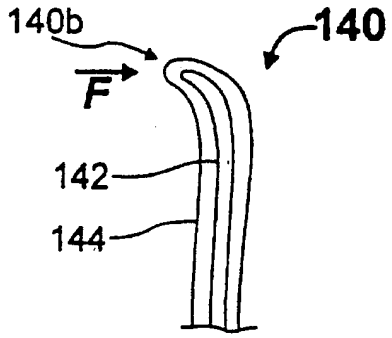


Figure 1E

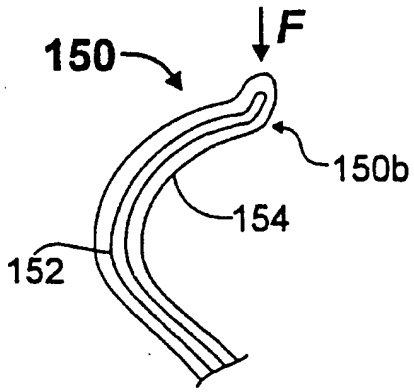


Figure 2A

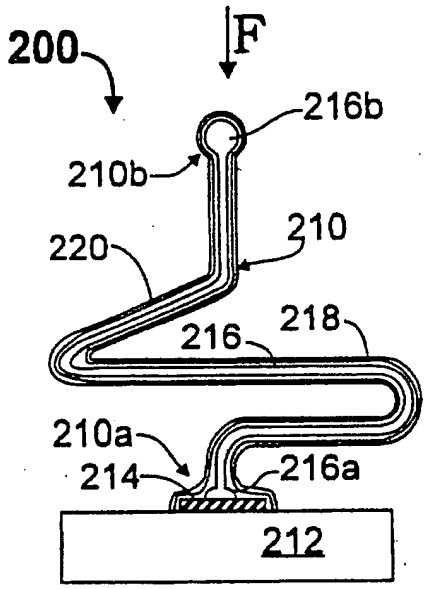


Figure 2B

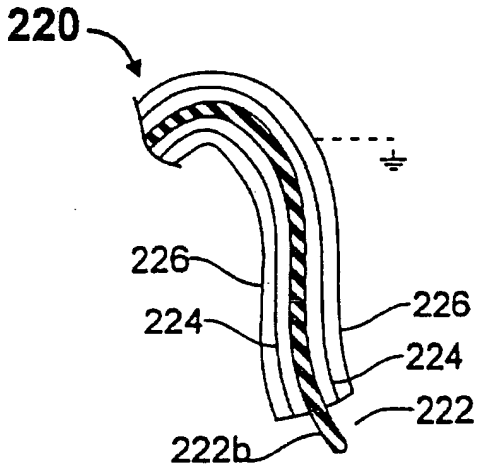


Figure 2C

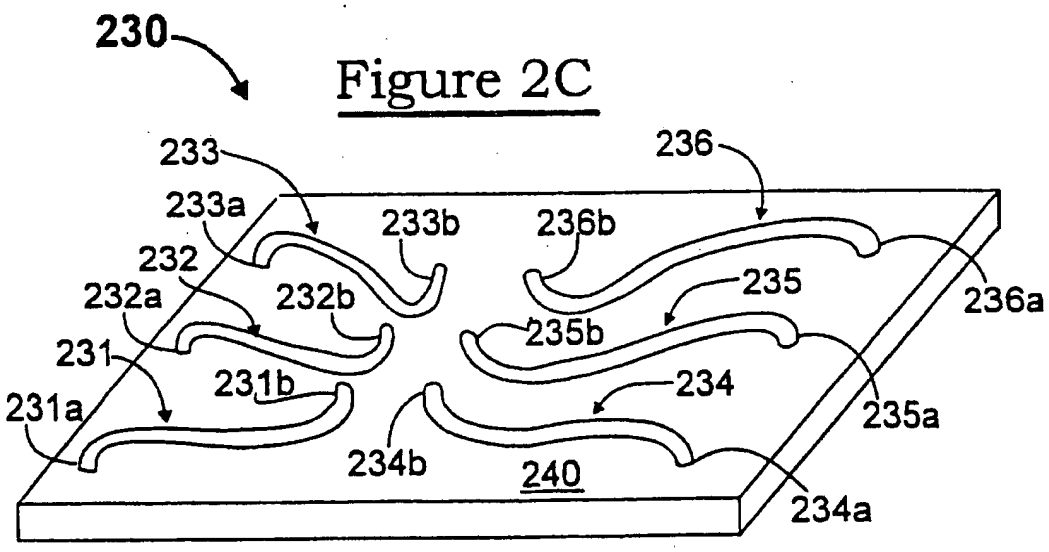


Figure 2D

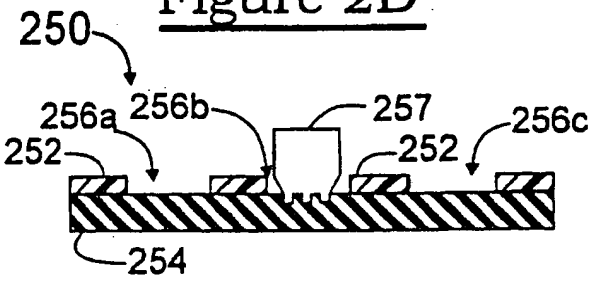


Figure 2E

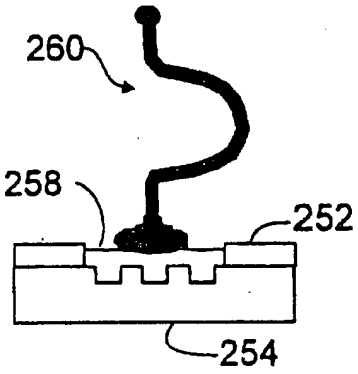


Figure 2F

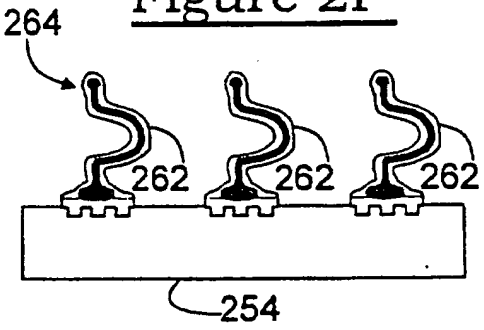


Figure 2G

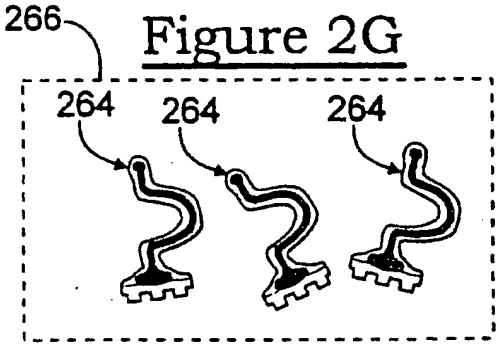


Figure 2H

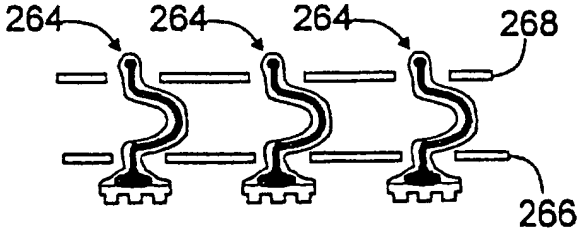


Figure 2I

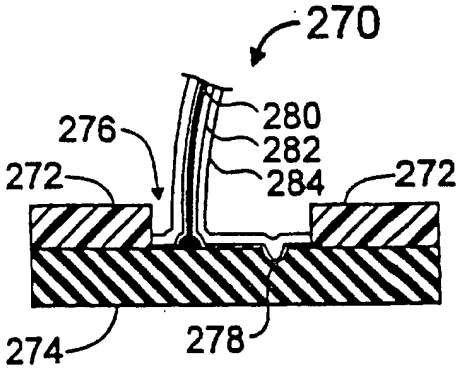


Figure 3

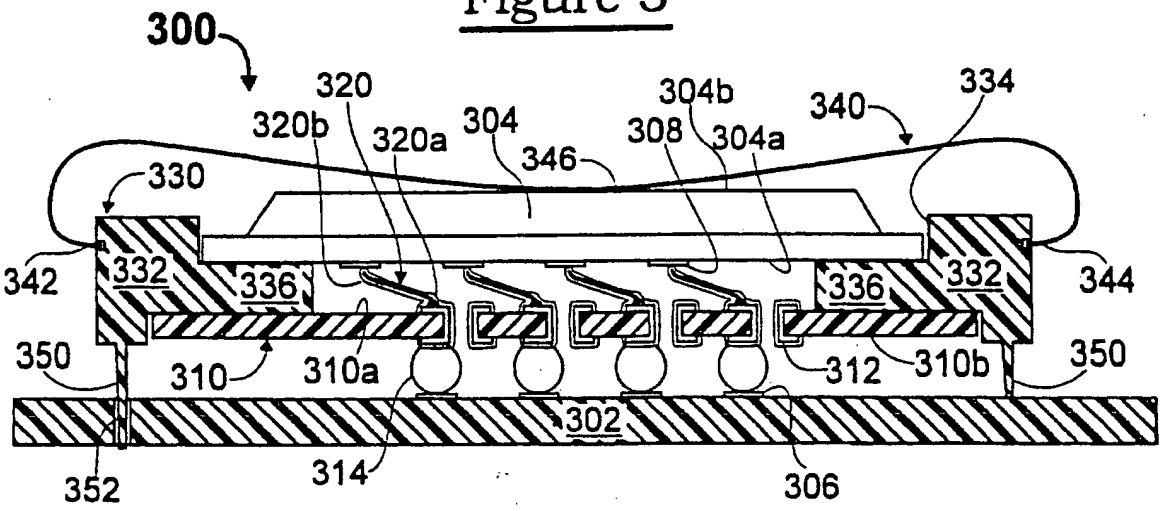


Figure 3A

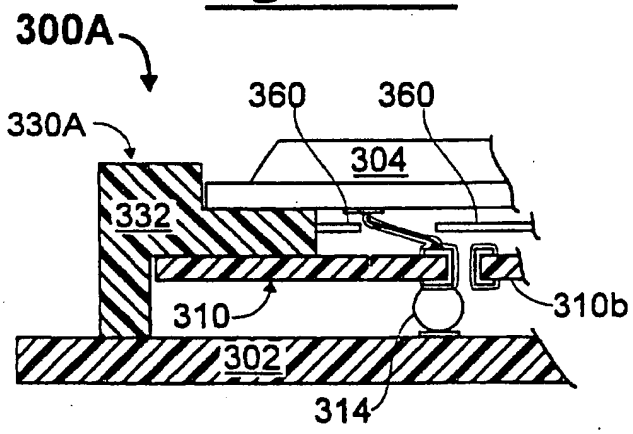


Figure 3B

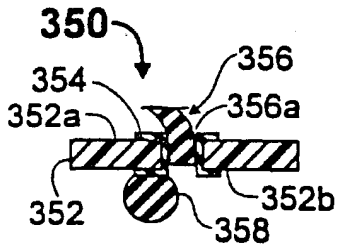


Figure 3C

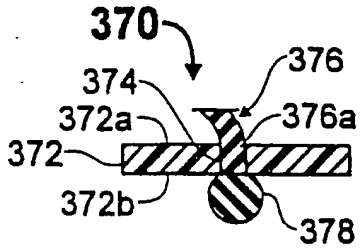


Figure 4

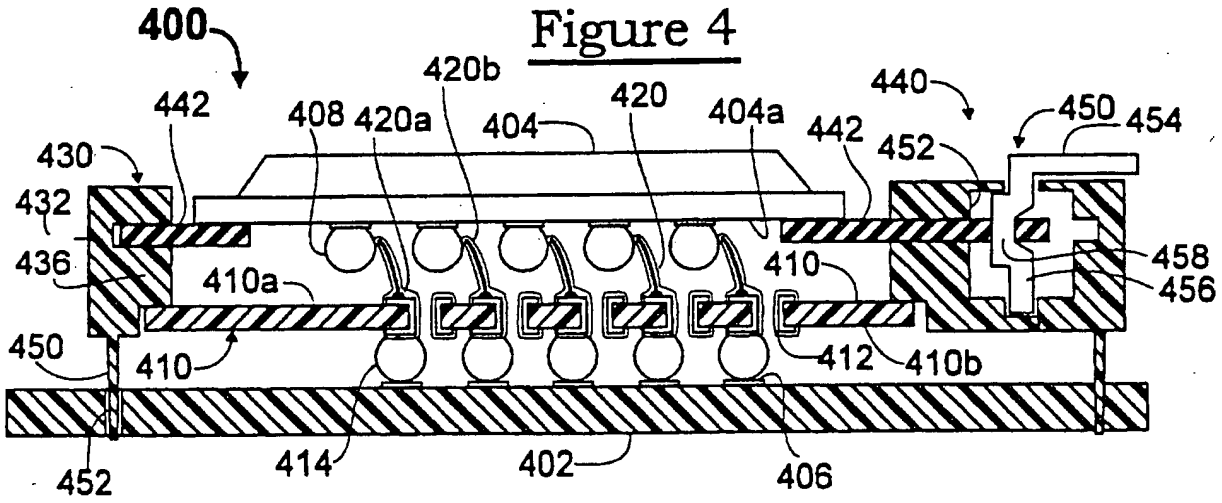


Figure 4A

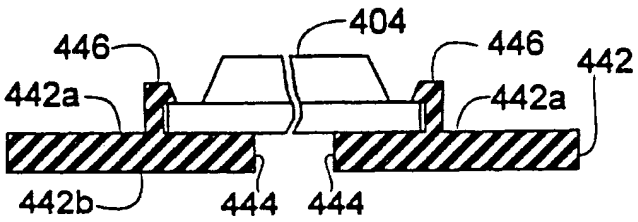


Figure 4B

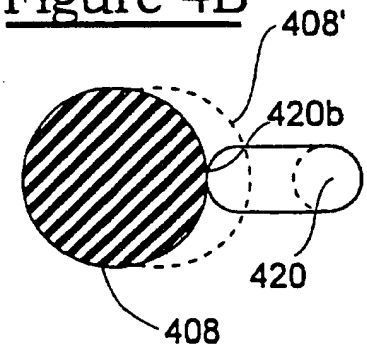


Figure 4C

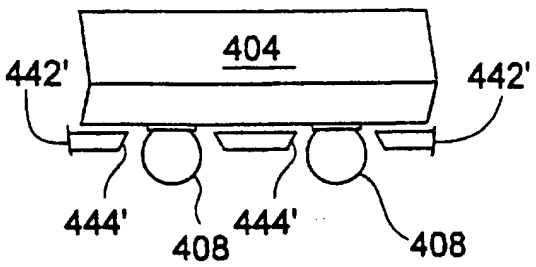


Figure 4D

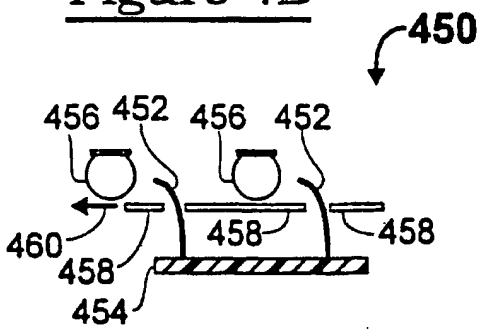


Figure 5A

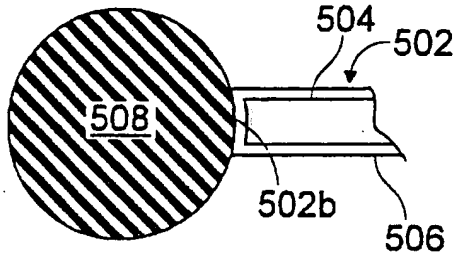


Figure 5B

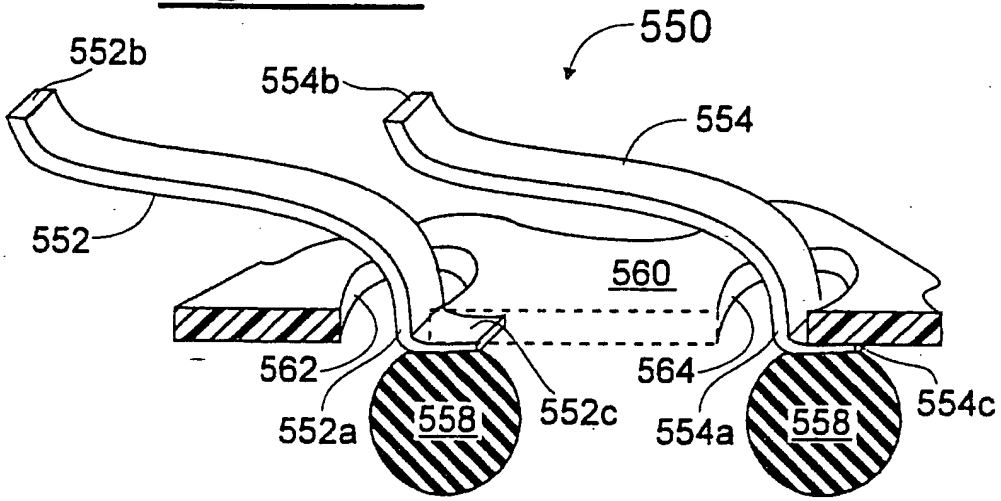


Figure 5C

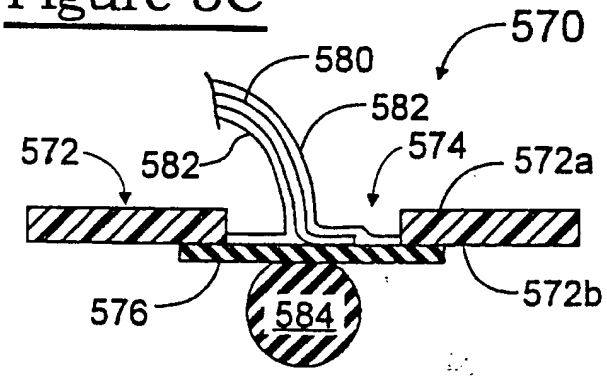


Figure 5D

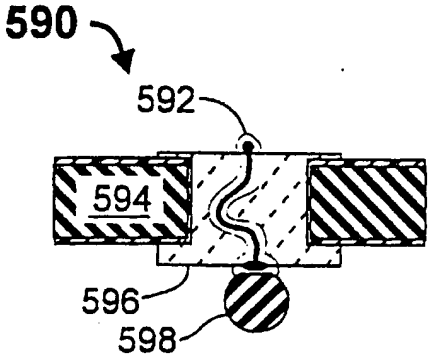


Figure 6A

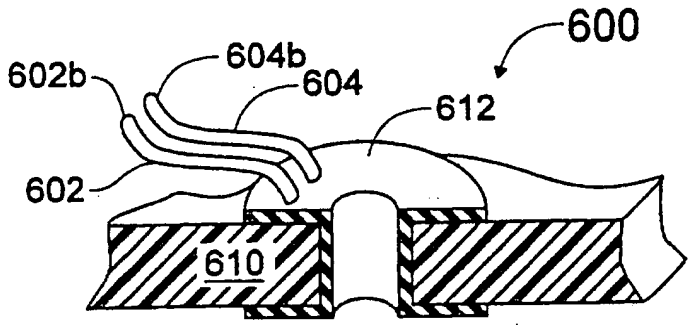


Figure 6B

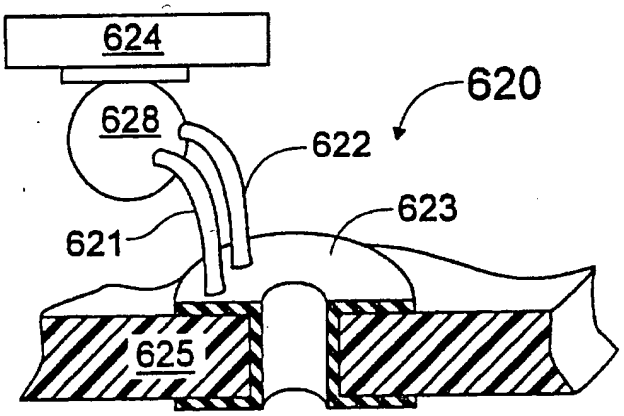


Figure 6C

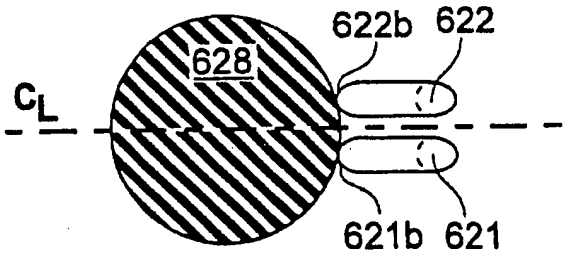


Figure 6D

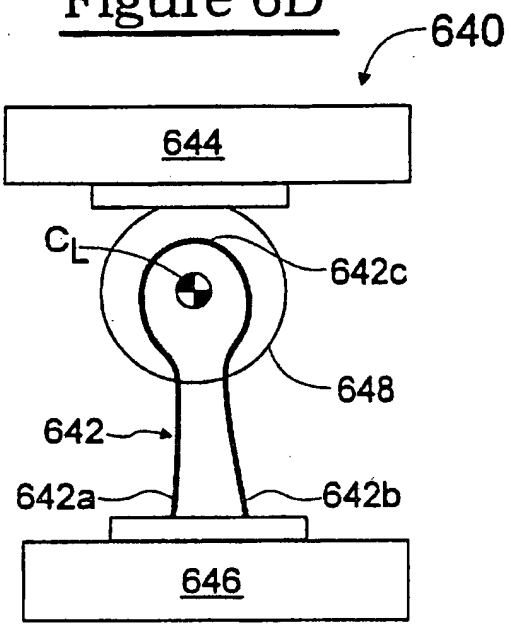


Figure 6E

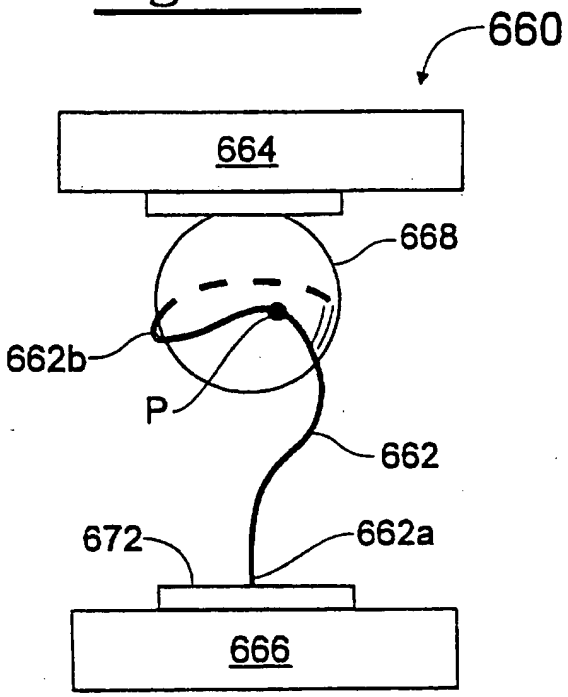


Figure 7A

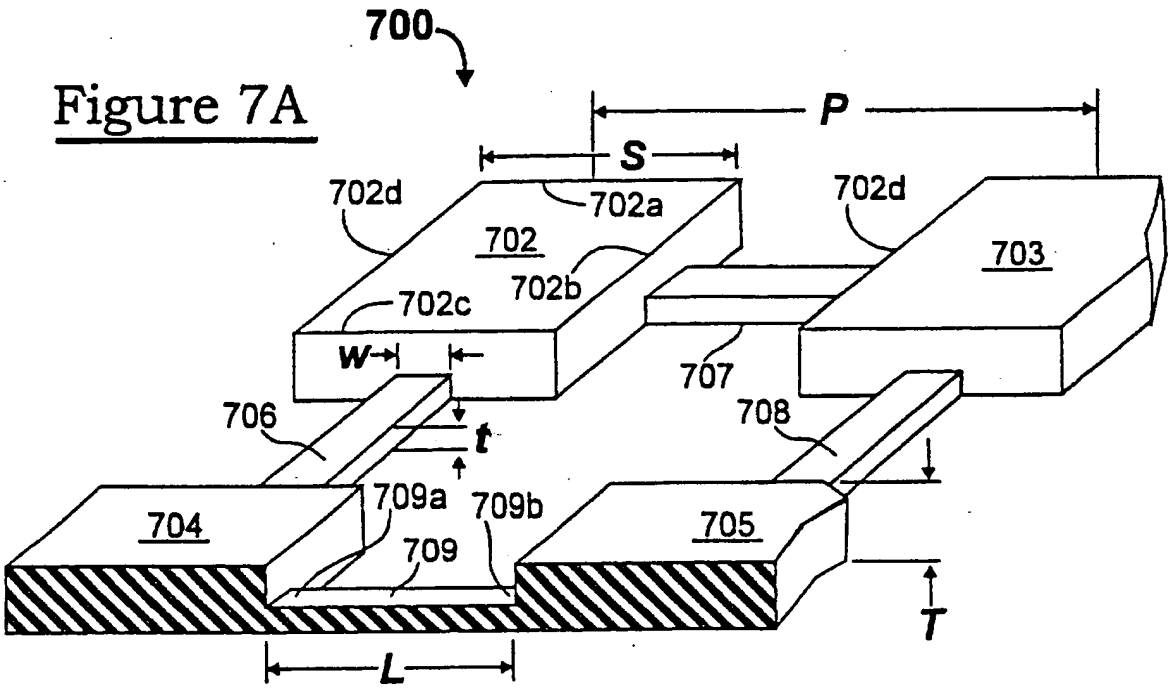


Figure 7B

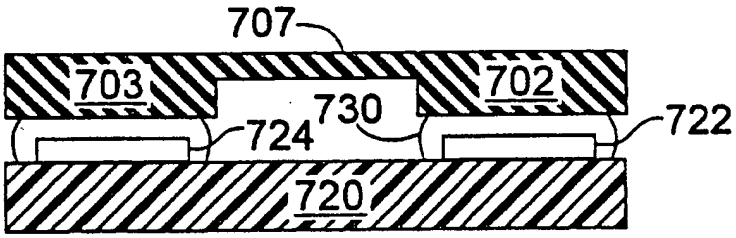
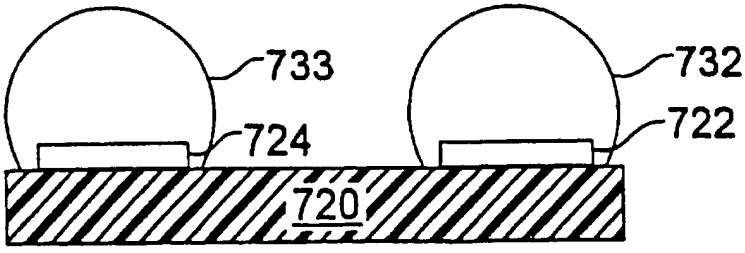


Figure 7C



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/14842

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/60, H01L 21/58 , H05H 1/18
US CL :29/830, 238/180.22, 257/693, 361/776
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 29/830, 831; 174/52.4; 228/56.3, 180.22, 185;257/693, 697, 698, 700, 713, 361/776, 813; 437/209, 220; 439/70, 81, 91,

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DIALOGUE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 3,509,270 (DUBE ET AL) 28 APRIL 1970	1-61
A	US, A, 3,616,532 (BECK) 02 NOVEMBER 1971	1-61
A	US, A, 4,074,342 (HONN ET AL) 14 FEBRUARY 1978	1-61
A	US, A, 4,418,857 (AINSLIE ET AL) 06 DECEMBER 1983	1-61
A	US, A, 4,667,219 (LEE ET AL) 19 MAY 1987	1-61
A	US, A, 4,705,205 (ALLEN ET AL) 10 NOVEMBER 1987	1-61
A	US, A, 4,764,848 (SIMPSON) 16 AUGUST 1988	1-61
A	US, A, 4,793,814 (ZIFCAK) 27 DECEMBER 1988	1-61

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 18 MARCH 1996	Date of mailing of the international search report 26 APR 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer for CARL J. ARBES Telephone No. (703) 308-1857 Sheila Veney Paralegal Specialist Group 3200

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/14842

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,860,433 (MIURA) 29 AUGUST 1989	1-61
A	US, A, 4,893,172 (MATSUMOTO ET AL) 09 JANUARY 1990	1-61
A	US, A, 5,045,975 (CRAY ET AL) 03 SEPTEMBER 1991	1-61
A	US, A, 5,067,007 (KANJI ET AL) 19 NOVEMBER 1991	1-61
A	US, A, 5,189,507 (CARLOMAGNO ET AL) 23 FEBRAURY 1993	1-61
A	US, A, 5,317,479 (PAI ET AL) 31 MAY 1994	1-61